



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Madan et al. Art Unit: 2818
Serial No.: 10/614,299 Examiner: Yoha, C.
Filing Date: 07/02/2003 Docket No.: TI-34844
Customer No.: 23494 Conf. No.: 8279

Title: CIRCUIT AND METHOD FOR REDUCING ACCESS TRANSISTOR GATE
OXIDE STRESS

TRANSMITTAL OF FORMAL DRAWINGS

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Attn: Official Draftsperson

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being
deposited with the U.S. Postal Service as First Class Mail
in an envelope addressed to: Commissioner of Patents,
P. O. Box 1450, Alexandria, VA 22313-1450.

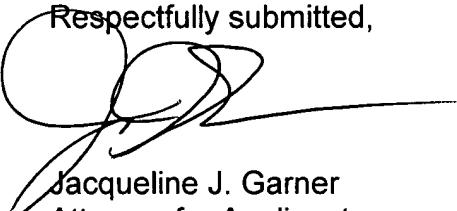
Date

9-10-04
Marianna Smith

Submitted herewith are five (5) sheets of formal drawings including the required
correction to Figure 8.

Charge any necessary fee to Deposit Account No. 20-0668. The original and a
copy of this authorization are enclosed.

Respectfully submitted,


Jacqueline J. Garner
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